

**REMARKS**

Claims 1-20 are pending in the present application. Claims 1, 2, 6-8, 12-14 and 18 have been amended.

**Election of Species Requirement**

In the Response to Election of Species Requirement dated October 13, 2004, Applicant asserted that claims 1-3, 5, 6, 13-15, 17 and 18 are generic to each of Species I – III identified in the Election of Species Requirement dated September 13, 2004. On page 2 of the current Office Action dated December 23, 2004, the Examiner has alleged responsive to this assertion by Applicant that “For example, claim 1 defines raised S/D electrodes made of polysilicon, which may not necessarily readable on the invention defined in claim 7 which recites raised S/D electrodes made of silicide”.

Applicant respectively emphasizes that claim 1 features in combination a polysilicon layer “formed on the source/drain region of the thin silicon layer”. Claim 7 features in combination a silicide layer “formed directly on the source/drain region of the thin silicon layer and the gate electrode”. Claim 1 does not specifically recite “raised S/D electrodes made of polysilicon”, and claim 7 does not specifically recite “raised S/D electrodes made of silicide”, as asserted by the Examiner.

Applicant further respectively submits that the above noted features of claim 7 as asserted by the Examiner, are irrelevant with respect to the issue of whether claims 1-3, 5, 6, 13-15, 17 and 18 are generic to each of Species I – III as respectively illustrated in

Figs. 3-11C, Figs. 12A-12C and Figs. 13A- 3C. That is, regardless of the scope of claim 7 as interpreted by the Examiner, it is Applicant's position that claims 1-3, 5, 6, 13-15, 17 and 18 are generic and thus readable on each of Species I – III.

Applicant however acknowledges that all of claims 1-20 have been examined in connection with the Office Action dated September 23, 2004.

### **Priority Under 35 U.S.C. 119**

Applicant notes the Examiner's acknowledgment of the Claim for Priority under 35 U.S.C. 119, and receipt of the certified copy of the priority document.

### **Claim Objections**

Claims 1-20 have been objected to because of the informalities as listed on page 3 of the current Office Action. This objection is respectfully traversed for the following reasons.

With regard to claims 1, 7 and 13, the Examiner has alleged that the present application, especially the drawings, features thin silicon layer 33 as having isolation layer 37 on the illustrated sides thereof only, instead of being surrounded so as to cover thin silicon layer 33 from all directions. Applicant respectfully submits that one of ordinary skill would readily understand the scope of original claims 1, 7 and 13 with regard to the isolation layer. Claim 1 has however been amended to feature that the isolation layer is "adjacent" the thin silicon layer, merely to expedite prosecution of this

application. Claims 13 and 17 have been amended in a somewhat similar manner. The Examiner is therefore respectfully requested to withdraw the objection to claims 1, 13 and 17.

The Examiner has asserted that the term "surrounds" in claims 2, 8 and 14 appears to be inappropriate. Applicant respectfully submits that one of ordinary skill would readily understand the scope of original claims 2, 8 and 14 with regard to the sidewall. Claims 2 has however been amended to feature that the sidewall is "adjacent" the gate electrode, merely to expedite prosecution of this application. Claims 8 and 14 have been amended in a somewhat similar manner. The Examiner is therefore respectfully requested to withdraw the objection to claims 2, 8 and 14.

Regarding claims 5, 11 and 17, as generally described on page 7, lines 4-7 of the present application, the thickness of SOI layer 8 in Fig. 1 is 20 to 80% the thickness of the source/drain portions, wherein the source/drain portions would include polysilicon layers 4A and 4B and the corresponding portions of SOI layer 8 that extend thereunder. This interpretation should be clear in view of Fig. 7B for example, wherein polysilicon layer 43 is shown as formed on SOI layer 33, to collectively form source/drain regions. Applicant therefore respectfully requests the Examiner to withdraw this objection of claims 5, 11 and 17.

Applicant also respectfully notes that the Examiner's comments with respect to claims 8 and 20 are unclear. Regarding claim 8 for example, although not necessarily limited thereto, sidewall 42 in Fig. 10C of the present application may be characterized

as formed on gate insulation layer 38 and as surrounding gate 40 and silicide layer 46. The Examiner is therefore respectfully requested to withdraw the objection to claims 8 and 20.

### **Claim Rejections-35 U.S.C. 102**

Claims 1-5, 7-11, 13-17, 19 and 20 have been rejected under 35 U.S.C. 102(b) as being anticipated by the Wakahara et al. reference (Japanese Patent Publication No. 2000-183355). This rejection is respectfully traversed for the following reasons.

The full depletion SOI-MOS transistor of claim 1 includes in combination a substrate; a buried oxide layer; a thin silicon layer "formed on the buried oxide layer, the thin silicon layer including a channel region and a source/drain region"; an isolation layer; a gate insulation layer; a gate electrode; and a polysilicon layer "formed on the source/drain region of the thin silicon layer". Applicant respectfully submits that the Wakahara et al. reference as relied upon by the Examiner does not disclose these features.

The Examiner has alleged that silicon layer 13b in Fig. 11 of the Wakahara et al. reference "is naturally a polysilicon since the nature of the deposition in which at least a portion of the silicon layer (13b) is deposited on the isolation layer (4)". Applicant respectfully disagrees for the following reasons.

As described in paragraph [0020] of the English translation of the Wakahara et al. reference with respect to Fig. 1, a **thin film silicon layer 3** that is p-type is formed

on oxide film 2. In contrast, as described in paragraph [0022] of the translation of the Wakahara et al. reference with respect to Fig. 2, polycrystalline silicon film 6 and silicon nitride film 7 are formed by chemical vapor growth (CVD) on gate dielectric film 5. Clearly, thin film silicon layer 3 in Fig. 1 of the Wakahara et al. reference is not polycrystalline silicon.

As described in paragraph [0029] of the translation of the Wakahara et al. reference with respect to Fig. 8, silicon 13a is formed by selective silicon growth on exposed polycrystalline silicon film 6, and silicon 13b is deposited on the front face of thin film silicon layer 3. Silicon 13b in Fig. 8 of the Wakahara et al. reference is not specifically described as polycrystalline silicon but is merely described as silicon growth, and thus cannot be interpreted as the polysilicon layer of claim 1 as alleged by the Examiner. As noted above, the Wakahara et al. reference makes clear distinction between polycrystalline silicon and other silicon layers. Since silicon 13b is not polysilicon, the MISFET of the Wakahara et al. reference does not have enhanced electron mobility with decreased source/drain resistance and increased on-current resistance as does the devices of the present application (see page 5, line 21 through to page 6, line 1 of the present application). The Wakahara et al. reference as relied upon by the Examiner clearly does not meet the features of claim 1. Applicant therefore respectfully submits that the full depletion SOI-MOS transistor of claim 1 distinguishes over the Wakahara et al. reference as relied upon by the Examiner, and that this rejection of claims 1-5 is improper for at least these reasons.

The full depletion SOI-MOS transistor of claim 7 includes in combination a substrate; a buried oxide layer; a thin silicon layer "formed on the buried oxide layer, the thin silicon layer including a channel region and a source/drain region"; an isolation layer; a gate insulation layer; a gate electrode; and a silicide layer "formed directly on the source/drain region of the thin silicon layer and the gate electrode". Applicant respectfully submits that the Wakahara et al. reference as relied upon by the Examiner does not disclose these features.

The Examiner has interpreted thin film silicon layer 3 as initially described with respect to Fig. 1 of the Wakahara et al. reference as the thin silicon layer of claim 7. The Examiner has further interpreted titanium silicide layer 15 as formed on silicon growth layer 13b in Figs. 10 and 11 of the Wakahara et al. reference as the silicide layer of claim 7. However, titanium silicide layer 15 is not formed directly on thin film silicon layer 3. The structure of the Wakahara et al. reference therefore fails to meet the features of claim 7. Applicant therefore respectfully submits that the full depletion SOI-MOS transistor of claim 7 distinguishes over the Wakahara et al. reference as relied upon by the Examiner, and that this rejection, insofar as it may pertain to claims 7-11, is improper for at least these reasons.

The full depletion SOI-MOS transistor of claim 13 includes in combination a substrate; a BOX layer; an SOI layer "formed on the BOX layer, the SOI layer including a channel region and a source/drain region"; an isolation layer; a gate insulation layer; a gate electrode; and a high mobility conductive layer "formed on the source/drain region

of the thin silicon layer, the high mobility conductive layer containing polysilicon”.

Applicant respectfully submits that the full depletion SOI-MOS transistor of claim 13 distinguishes over the Wakahara et al. reference as relied upon by the Examiner for at least somewhat similar reasons as set forth above with respect to claim 1. Silicon 13b of the Wakahara et al. reference is not described as a high-mobility conductive layer containing polysilicon. Accordingly, Applicant respectfully submits that this rejection of claims 13-17, 19 and 20 is improper for at least these reasons.

#### **Claim Rejections-35 U.S.C. 103**

Claims 6, 12 and 18 have been rejected under 35 U.S.C. 103(a) as being unpatentable over the Wakahara et al. reference in view of the Cheng et al. reference (U.S. Patent Application Publication No. 2002/0171107). Applicant respectfully submits that the Cheng et al. reference as relied upon by the Examiner does not overcome the above noted deficiencies of the Wakahara et al. reference.

#### **Conclusion**

Applicant respectfully submits that claims 1, 6, 12, 13 and 18 have been amended merely responsive to the claim objections, not to substantively change claim scope. Accordingly, these corresponding amendments should not be construed as narrowing scope within the meaning of *Festo*.

The Examiner is respectfully requested to reconsider and withdraw the

corresponding rejections, and to pass the claims of the present application to issue, for at least the above reasons.

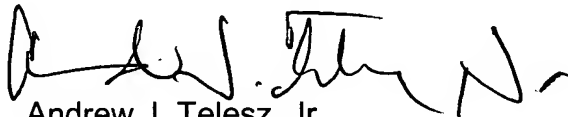
In the event that there are any outstanding matters remaining in the present application, please contact Andrew J. Telesz, Jr. (Reg. No. 33,581) at (571) 283-0720 in the Washington, D.C. area, to discuss these matters.

Pursuant to the provisions of 37 C.F.R. 1.17 and 1.136(a), the Applicant hereby petitions for an extension of two (2) months to May 23, 2005, for the period in which to file a response to the outstanding Office Action. The required fee of \$450.00 should be charged to Deposit Account No. 50-0238.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment for any additional fees that may be required, or credit any overpayment, to Deposit Account No. 50-0238.

Respectfully submitted,

VOLENTINE FRANCOS & WHITT, P.L.L.C.

A handwritten signature in black ink, appearing to read 'Andrew J. Telesz, Jr.', with a stylized flourish at the end.

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